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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,368	07/18/2003	Celine Mas	S1022.81025US00	5360

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EXAMINER	
SHERMAN, STEPHEN G	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/622,368	MAS ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/27/03, 7/18/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

Page 1, lines 22-23 read: "...which injects or not a current into each electrode column to turn on or not the column pixel." The examiner suggests: "...which injects or doesn't inject a current into each electrode column to turn on or to not turn on the column pixel."

Page 6, line 18 reads: "Reading interface 22 is connected..." The examiner suggests: "Writing interface 22 is connected..."

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Aratani et al. (US 5,929,831).

Regarding claim 1, Aratani et al. disclose:

a method for displaying an image on an array screen by activation of screen pixels arranged in rows and columns (Column 4, lines 45-59),

each pixel of a same row corresponding to a memory point of a same row of a memory (Column 5, lines 35-40),

said memory point being set to an activation state when the corresponding pixel is to be activated (Column 5, lines 35-40), comprising the steps of:

identifying, among sets of memory rows, the row sets for which at least one memory point of a row of the set is at the activation state (Figure 6, S1-1 and S1-2 and column 6, lines 27-37);

determining a read clock signal based on the number of sets of identified rows and successively selecting at the frequency of said read clock signal the only lines corresponding to the rows of the sets of rows identified for the pixel activation (Column 8, lines 8-23. The examiner interprets that in the case of the embodiment where lines are skipped, that the frequency calculated by the formula is the frequency of a read clock signal, which is shown in the formula to be based on the number of flags, i.e. identified rows, and that since the data is rewritten, at the frequency calculated, the examiner interprets that the scanning lines identified by the flags are the lines selected at the found frequency.).

Regarding claims 2 and 3, Aratani et al. disclose the method of claim 1. Aratani et al. also disclose wherein the first step comprises the steps of:

setting, for each row of the memory, a memory point of an auxiliary memory to the activation state if one or at least one memory point of the row is at the activation state (Figure 6, S1-2 and column 6, lines 27-33);

determining the memory points of the auxiliary memory at the activation state (Figure 6, S1-5. The examiner interprets that checking to see if the flag is set would determine whether the memory is designated or not.); and

identifying the row blocks corresponding to said memory points of the auxiliary memory in the activation state (Figure 7. Memory 27 is the auxiliary memory, which can be seen with "1's" designating the scan lines of the memory points needed to be scanned and the corresponding rows are identified with cross-hatching as explained in column 7, lines 20-30.).

Regarding claim 4, Aratani et al. disclose the method of claim 3. Aratani et al. also disclose the method further comprising the steps of:

reading, for each selected row, the states of the memory points of the selected row and setting a memory point of the auxiliary memory to the deactivation state if all the memory points of the row are in the deactivation state (Column 7, lines 23-27. The examiner interprets that the flag in the memory not being set is the same as the memory being set to the deactivation state, and that the flag isn't set unless there is a memory point activated.).

Regarding claim 5, Aratani et al. disclose the method of claim 1. Aratani et al. also disclose wherein the frequency of the read clock signal multiplied by the total number of rows of the sets of identified rows is substantially constant (Column 8, lines 8-20. 56 Hz is the frequency of the read clock and the number of flags id equal to the total number of rows of the sets of identified rows. When the formula is rearranged it equals: [56 Hz (frequency of the clock) x the number of flags = 20 Hz x the number of scanning lines], which is constant.).

Regarding claim 6, Aratani et al. disclose the method of claim 1. Aratani et al. also disclose wherein when a set of rows has contained at least one memory point in the activation state for the display of a determined image, the lines of the screen corresponding to said set of rows are selected, at least for the display of the next image, even if all the memory points of said set of rows are in the deactivation state (Column 6, lines 31-33. The examiner interprets that since any time the information is updated the flag is set, that when the row was in the activation state and then is set to the deactivation state, that this constitutes as updating the information and that the lines of the row would be selected even if all of the pixels were deactivated.).

Regarding claim 7, Aratani et al. disclose:

a device for displaying an image on an array screen by activation of screen pixels arranged in lines and columns (Column 4, lines 45-59), comprising:

a main memory (Figures 2 and 5, item 26 video memory), each pixel of a same screen line corresponding to a memory point of a same row of the main memory, said memory point being set to an activation state when the corresponding pixel is to be activated (Column 5, lines 35-40);

an addressing means for successively providing row addresses of the main memory (Figure 3, address generation unit 44);

a read means (Figures 3 and 4, selector 46), receiving said successive row addresses, and adapted to read, for each address, the states of the memory points of the corresponding row;

a row driver for selecting screen lines based on the addresses (Figure 2, Driver IC 23); and

a column driver for activating pixels of the selected lines (Figure 2, Driver IC 22), comprising

a means for identifying, among sets of memory rows, sets of rows for which at least one memory point of a row in the set being in the activation state (Figure 3, partially rewriting area detection unit 33), a means for providing a read control signal transmitted to the addressing means (Figure 2, panel drive controller provides graphic and display controller, which contains the address generation unit (as shown in Figure 3), with control signals Sync and Pst.), the frequency of which depends on the total number of rows of the identified row sets and wherein the addressing means is adapted to successively providing the row addresses of the identified row sets at the frequency of the read control signal (Column 8, lines 8-20.).

Regarding claim 8, Aratani et al. disclose the device of claim 7. Aratani et al. also disclose the device further comprising an auxiliary memory (Figures 2 and 5, memory for scanning area designation 27) connected to the identification means (Figure 3, memory for scanning area designation 27 is connected to the partially rewriting area detection unit 33) and each memory point of which is associated with a row of the main memory (Figure 5, memory 27 can be seen to be associated with the rows of video memory 26) and is in the activation state if a memory point of the corresponding row is in the activation state (Figure 7, the memory flag can be seen to be set to "1" when the corresponding row is in the activation state shown by the cross-hatching.).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kanno et al. (US 5,726,679) discloses a display that supplies address data to only the scanning lines corresponding to change in display data.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

28 November 2005